



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,499	09/30/2003	Motoki Kobayashi	FUJI I37	2321
23995	7590	05/04/2005	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			ROSE, KIESHA L	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/673,499	KOBAYASHI ET AL.	
	Examiner Kiesha L. Rose	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 07 February 2005.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-8 and 10 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date: _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

This Office Action is in response to the amendment filed 7 February 2005.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Independent claim 1 discloses a target element "whose dielectric loss is to be controlled among the at least one element" this claim is unclear in regards to the how the target element has a dielectric loss and if the at least one element is controlling its dielectric loss how is it doing that. In regards to claim 6, it is unclear how the analog element is an element that controls its dielectric loss it is unclear how the dielectric loss is achieved.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,5-7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonehara et al. (U.S. Patent 5,530,266).

Yonehara discloses a semiconductor device (Figs. 15G and 38) that contains a silicon support substrate (61/44), an insulation layer (62/45) on top of the supporting substrate, an SOI layer (71/42) formed on top of the insulation layer, at least one analog element (transistor) (55/56/57/47) formed on the SOI layer and at least one groove (84) formed in the supporting substrate such that a reverse face of the insulation is exposed and being located below a target element (57) whose dielectric loss is to be controlled among the elements.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara in view of Eda et al. (U.S. Patent 5,668,057).

Yonehara discloses all the limitations except for the analog element to be an inductor. Whereas Eda discloses a semiconductor device (Fig. 6) that contains a supporting substrate (1) with analog elements (3-5) are formed thereon where the analog element is an inductor or a transistor. An inductor is used as a passive chip component. (Column 13, lines 25-30) Therefore it would have been obvious to one

having ordinary skill in the art at the time the invention was made to have that analog element to be an inductor to act as a passive chip component as taught by Eda.

***Response to Arguments***

Applicant's arguments filed 7 February 2005 have been fully considered but they are not persuasive. Applicant argues that the prior art references do not disclose the dielectric loss, whereas the dielectric loss is dependent on the substrate and as stated in the abstract and the specification of the application (Page 4, 1<sup>st</sup> paragraph) that the dielectric loss is dependent on the substrate and the dielectric loss is achieved for an element anywhere that a groove is located in the substrate under the element. Therefore the transistor in the Yonehara has a groove in the substrate under the transistor therefore there would be dielectric loss of the element. In addition since the substrate is etched back to the dielectric layer of the SOI then the dielectric loss would be achieved since the dielectric layer does not have a layer underneath. Therefore the rejection stands.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KR  
KLR



AMIR ZARABIAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800